SCOPE OF THE HIGH-END WORKSHOP(KARYASHALA)

VLSI (Very Large Scale Integration) design is an important field that deals with the design and fabrication of integrated circuits. The proposed workshop provides students and professionals with the necessary skills and knowledge to work in the field of VLSI design.

The scope of this workshop is to deliver the design aspects and provide hands-on experience with VLSI design tools such as Vivado (Xilinx) and Cadence in the following domains:

- **Digital Design:** Digital design concepts including combinational and sequential logic, finite state machines, and basic digital circuits.
- **Analog Design:** Analog design concepts including basic amplifier design, filters, and analog-to-digital conversion.
- **Advanced Topics in VLSI Design**: Recent advancements in VLSI design such as low-power design, high-speed design, and mixed-signal design.

WORKSHOP OBJECTIVES

- Participants will get an extensive knowledge of the basic ideas and concepts of VLSI design, including digital logic design, circuit modelling, timing analysis, power optimization, and integrated circuit (IC) fabrication procedures.
- Participants will be introduced to industry-standard tools such as Xilinx and Cadence, which are widely used in the VLSI design flow.
- The workshop will cover techniques for optimizing the performance of VLSI circuits, including power consumption, area utilization, and timing constraints.
- Participants should learn about the synthesis process, which involves converting the high-level design into a gate-level representation suitable for manufacturing.
- Participants will work on real-world projects or case studies to apply their newly acquired skills and knowledge.
- The workshop will provide an environment for participants to collaborate, share ideas, and network with fellow attendees and experts in the field.

WHO CAN ATTEND

- The workshop is open for Research Scholar/PG/UG(Final Year) students from all Institutes and Universities.
- Preference will be given to the students having interest towards Electronics, VLSI, Embedded Systems, Artificial Intelligence and Machine Learning Applications, HDL – Verilog, FPGA implementation.
- Total number of seats is **limited to *25***.
- The participants will be selected based on their academic/research credentials and first-come-first-serve basis.
- The selected applicants will be provided food & accommodation at IIIT Una.
- The traveling expenses (upto 3AC) will be reimbursed as per the SERB guidelines.

REGISTRATION LINK

https://bit.ly/VCSXC

REGISTRATION PROCEDURE

- Only selected candidates will be informed by email/ phone, therefore the candidates must provide valid E-mail IDs and phone while doing the online registration.
- The selected candidates will have to acknowledge and accept the offer for participating in the workshop through return email, failing which the wait-listed candidates may be called for the workshop.

IMPORTANT DATES

Registration Opens :	*09* February, *2024*
Last date for Application :	*04 March, 2024*
Display of shortlisted candidates :	*05* March, *2024*
Workshop Dates :	16-22 *March, 2024*

CERTIFICATION

Certificate will be provided to the participant upon successful completion of the workshop with 100% attendance and securing a minimum of 60% marks in quiz.

Indian Institute of Information Technology Una
Himachal Pradesh
(An Institute of National Importance under MoE)

High-End Workshop (Karyashala)

On

Hands-on Workshop on VLSI Circuits and Systems using Xilinx and Cadence Tools

16- 22 March, 2024

Sponsored by:

Science and Engineering Research Board (SERB), DST, GoI

Under the Accelerate Vigyan Scheme

Organized by:

School of Electronics

Indian Institute of Information Technology Una

Himachal Pradesh-177209

ABOUT IIIT UNA

IIIT Una is one of the 20 IIITs being set up, funded, and managed by the MoE, GoI, under the Public-Private Partnership (PPP) model in the year 2014, an Institute of National Importance (INI) by an Act of Parliament, GoI. The partners involved in setting up IIIT Una are the Ministry of Education, Government of India, the Government of Himachal Pradesh, HP Power Corporation Limited, and HP Power Transmission Corporation Limited. Admissions to the undergraduate programs at the Institute are made through the Joint Entrance Examination (JEE) Main.

SCHOOL OF ELECTRONICS (SOE)

The School of Electronics, established in 2014, offers UG, PG, and PhD programs in Electronics and Communication Engineering. With expertise in VLSI, Communication, RF, Signal processing, it has various software like Cadence Virtuoso, Xilinx Vivado, MATLAB, CST Studio, alongside PCB design and fabrication facilities, fostering technical sessions and expert talks periodically.

ABOUT SERB, KARYASHALA

Science and Engineering Research Board is a statutory body under the Department of Science and Technology, Government of India, established by an Act of the Parliament of India in 2009. The Board is chaired by the Secretary to the Government of India in the Department of Science and Technology.

'KARYASHALA' is an effort to improve research productivity of promising PG and PhD students from universities and colleges through high-end workshops on specific themes. This program aims to provide opportunities to acquire specialized research skills. These workshops will primarily be facilitated at organizations / institutions / laboratories of national importance such as IITs, IISc, IISERs, NITs, CSIR, ICAR, ICMR etc.

CHIEF GUEST - INAUGURATION

Prof. R. K. Nagaria
Professor, MNNIT Alllahabad

CHIEF GUEST - VALEDICTORY

Prof. Brajesh Kumar Kaushik
Professor, IIT Roorkee

RESOURCE PERSONS

- Prof. R. K. Sharma, Professor, NIT Kurukshetra
- Prof. M. Bhaskar, Professor, NIT Tiruchirappalli
- Prof. Manoj Kumar, Professor, NIT Delhi
- Dr. Gargi Khanna, Associate Professor, NIT Hamirpur
- Dr. Balwinder Raj, Associate Professor, NIT Jalandhar
- Dr. Ashish Raman, Associate Professor, NIT Jalandhar
- Dr. Hitesh Srimali, Associate Professor, IIT Mandi
- Dr. Ambika Prasad Shah, Assistant Professor, IIT Jammu
- Dr. Pradeep Duhan, Assistant Professor, IIT Ropar
- Dr. Mahendra Sakare, Assistant Professor, IIT Ropar
- Dr. Gaurav Saini, Assistant Professor, NIT Kurukshetra
- Dr. Trailokya Nath Sasamal, Assistant Professor, NIT Kurukshetra
- Mr. Anish. K. Sharma, Sr. FAE, Entuple Technologies Pvt. Ltd. Bangalore, KA, India.

TOPICS

- Design and analysis of Low Power Systems using Verilog
- Spintronics-Perspectives and Challenges
- Low Power Static and Dynamic CMOS Circuit Design
- Low Power Voltage Controlled Oscillator Design for Communication systems
- Design and Analysis of Low Power VLSI Circuit for Biomedical Applications
- CMOS Oscillator design and future trends
- In-memory computing for Edge AI Devices
- HfO2 based Ferroelectric Memory Devices
- High speed circuit design techniques using Cadence
- Low power device-circuit co-design: HDL Perspective (Hands-on Xilinx)
- Piezoelectric material-based MEMS Acoustic Sensors using Cadence
- Design and analysis of digital and analog circuits (Hands-on Cadence)
- Layout design of Digital Circuit (Hands-on Cadence)

PATRON

Prof. Binod Kumar Kanaujia, Director, IIIT Una

CONVENOR

Dr. Ankur Kumar, SoE
Dr. Naman Garg, SoE

COORDINATOR

Dr. Tanu Wadhera, SoE
Dr. Mrityunjay Singh, SoC

CO-COORDINATOR

Dr. Shatrughan Modi, SoC
Dr. Vejandla Kishore, SoE

ORGANIZING COMMITTEE

Dr. Naveen Cheggoju, SoE
Dr. Vikram Kumar, SoC
Dr. Shonal Chouksey, SoE
Dr. Sanjit Ningthoujam, SoC
Dr. Nishtha Hooda, SoC
Dr. Ashwani Malviya, SoC
Dr. Shivdutt Sharma, SoC
Dr. Ankur Thakur, SoE
Dr. Akhil Walia, SoE
Dr. Nikunj Goyal, SoE
Dr. Gridhar Gopal, SoE
Mr. Satish Kumar, SoE
Mr. Divyansh Thakur, SoC
Ms. Laxmanika, SoC
Ms. Pranshu Sharma, SoE

ADDRESS FOR CORRESPONDENCE

Dr. Ankur Kumar
Assistant Professor, SoE
Contact No.- +91-9837012205
Email: ankur@iiitu.ac.in