Dr. Ankur Kumar

B. Tech, M. Tech, Ph.D (Microelectronics & VLSI Design).

Affiliation: Assistant Professor
School of Electronics
Indian Institute of Information Technology (IIIT) Una
Saloh, Una, Himachal Pradesh-177209

Phone No.: 9837012205
E-mail: ankur@iiitu.ac.in, ankur.lamba10@gmail.com

Area of Specialization: Low Power VLSI Design, FET Biosensor.

Academic Credentials:

Qualification	Board/University	Year	Percentage
Ph.D	M. N. National Institute of Technology Allahabad	22 October, 2020	9.75 CGPA
M. Tech (Microelectronics & VLSI Design)	M. N. National Institute of Technology Allahabad	2016	9.20 CGPA
B. Tech (Electronics & Communication)	AKGEC, Ghaziabad (U.P.T.U Lucknow)	2014	73.33%

Dissertations:

- Ph.D dissertation submitted on "**Studies of Leakage and Variation Tolerant Wide Fan-in OR Logic Domino Circuits for Low Power VLSI Design**".
- M.Tech dissertation submitted on "Logical Effort Method for Dynamic Power and Delay Estimation in Low Power VLSI".
- B.Tech final-year project submitted on "METRO Rail : Auto Stop + Auto Reverse + Station Name Display + Door Opener".

Work Experience:

S. No.	Period		Position Held	Organization	Nature of work
	From	To			
1.	01-09-2021	30-04-2022	Assistant Professor	Institute of Engineering and Technology Lucknow	Teaching and Research
2.	03-11-2020	31-08-2021	Assistant Professor	Meerut Institute of Engineering and Technology, Meerut.	Teaching and Research

Research Publication:

Research Article: SCI Journals: **03** (Published/ Accepted)
Book Edited: **01**
Book Chapter: **07**
International Conference: **14**

Published/Accepted International SCI Research papers:

1. **Ankur Kumar** and R. K. Nagaria, "A Novel Method to Control Leakage and Noise in Domino Circuit for Wide Fan-In OR Logic," Journal of Circuits, Systems, and Computers, Vol. 31, No.4. 17 September 2021 **(ISSN-1793-6454)** https://doi.org/10.1142/S0218126622500554
2. **Ankur Kumar** and R. K. Nagaria, "A new process variation and leakage-tolerant domino circuit for wide fan-in OR gates," Analog Integrated Circuits and Signal Processing, Vol. 102, 9-25, 2020. (15-06-2019) (**ISSN- 1573-1979**) https://doi.org/10.1007/s10470-019-01473-3
3. **Ankur Kumar** and R. K. Nagaria, "A new leakage-tolerant high speed comparator based domino gate for wide fan-in OR logic for low power VLSI circuits," Integration The VLSI Journal, Vol. 63, 174-184, 16-07-2018. **(ISSN- 0167-9260)** https://doi.org/10.1016/j.vlsi.2018.07.004

Book Edited:

1. **Ankur Kumar**, Sajal Agarwal, Vikrant Varshney, Varun Mishra, Yogesh K. Verma and Suman Lata Triphati "**Opto-VLSI Devices and Circuits for Biomedical and Healthcare Applications**" CRC Series, Taylor and Francis. **(Book Proposal Accepted)**

Paper Publications in Book Chapters:

1. **Ankur Kumar**, Sajal Agarwal, Vikrant Varshney, Abhilasha Jain and R. K. Nagaria, " A Study of Leakage and Noise Tolerant Wide Fan-in OR Logic Domino Circuits", Nanotechnology: Device Design and Applications, CRC Series, Taylor and Francis, pp. 203-226. **(ISBN-9781003220350) (DOI- 10.1201/9781003220350-12)**
2. Sajal Agarwal,Yogendra Kumar Prajapati, and Ankur Kumar. "Advanced Materials-Based Nano-absorbers for Thermo-Photovoltaic Cells." Advances in Terahertz Technology and Its Applications. Springer, Singapore, 2021. Pp. 191-209. **(ISBN-978-981-16-5731-3) (DOI-10.1007/978-981-16-5731-3_11)**
3. Priyanka Singh, Vikrant Varshney, **Ankur Kumar**, and R. K. Nagaria "DV-EXCCCII based Electronically Tunable Current mode filter", Recent Trends in Electronics and Communication, Springer (20-01-2022), pp. 232-245. **(ISBN-978-981-16-2761-3) (DOI-https://doi.org/10.1007/978-981-16-2761-3_22)**
4. Priyanka Singh, Vikrant Varshney, **Ankur Kumar**, and R. K. Nagaria "DV-EXCCCII based Electronically Tunable Voltage Mode All Pass Filter", Recent Trends in Electronics and Communication, Springer (20-01-2022), pp. 485-494. **(ISBN-978-981-16-2761-3) (DOI- https://doi.org/10.1007/978-981-16-2761-3_43)**

5. Avaneesh K. Dubey, Vikrant Varshney, **Ankur Kumar**, Pratosh K. Pal and R. K. Nagaria "Low-Power Enhanced Speed Two-Tail Dynamically Controlled Comparator Suitable for Subthreshold CMOS Circuits", Recent Trends in Electronics and Communication, Springer (20-01-2022), pp.1121-1135. **(ISBN-978-981-16-2761-3) (DOI-https://doi.org/10.1007/978-981-16-2761-3_97)**
6. **Ankur Kumar**, Pratosh K Pal, Vikrant Varshney, Avaneesh K. Dubey, and R. K. Nagaria "Leakage tolerant low power wide fan-in OR-logic domino circuit", Advances in VLSI, Communication, and Signal Processing, pp 631-642, 15 October 2020. Springer. **(Presented)** (ISBN- 978-981-15-6840-4) https://doi.org/10.1007/978-981-15-6840-4_52
7. Avaneesh K. Dubey, Vikrant Varshney, **Ankur Kumar**, Pratosh K Pal, and R. K. Nagaria "Design and performance of High-Speed CMOS Double tail Dynamic Comparator suitable for Mixed-Signal ICs", Advances in VLSI, Communication, and Signal Processing, pp 75-87, 15 October 2020, Springer. (ISBN- 978-981-15-6840-4) https://doi.org/10.1007/978-981-15-6840-4_7

Paper Publications in International Conferences:

1. **Ankur Kumar**, Avaneesh K. Dubey, Vikrant Varshney, Priyanka Singh and R. K. Nagaria "A Hybrid Technique to Minimize the Leakage of Wide Fan-in OR-logic Domino Circuit", 3rd International Conference on VLSI, Communication and Signal Processing (VCAS 2020), 9-11 October 2020, MNNIT Allahabad, Prayagraj, UP, India. **(Accepted) (Presented)**
2. Priyanka Singh, Vikrant Varshney, **Ankur Kumar**, and R.K. Nagaria, "Electronically Tunable First Order Universal Filter based on CCDDCCTA", 3rd IEEE Conference on Information and Communication Technology (CICT 2019), 6-8 December 2019, IIIT Allahabad, UP, India. **(ISBN-978-1-7281-5398-8)** 10.1109/CICT48419.2019.9066264
3. Avaneesh K. Dubey, Pratosh K Pal, Vikrant Varshney, **Ankur Kumar**, and R. K. Nagaria, "Impact of Channel Doping Fluctuation and Metal Gate Work Function Variation in FD-SOI MOSFET for 5nm BOX Thickness", 3rd IEEE Conference on Information and Communication Technology (CICT 2019), 6-8 December 2019, IIIT Allahabad, UP, India. **(ISBN-978-1-7281-5398-8)** 10.1109/CICT48419.2019.9066255
4. **Ankur Kumar**, Vikrant Varshney, Priyanka Singh, and R.K. Nagaria, "A variation and noise tolerant wide fan-in OR-Logic Domino circuit", 6th IEEE Uttar Pradesh Section International Conference on Electrical, Computer and Electronics (UPCON), 8-10 Nov 2019, Aligarh Muslim University, UP, India. **(ISBN- 978-1-7281-3455-0) (Presented)** 10.1109/UPCON47278.2019.8980259
5. Vikrant Varshney, **Ankur Kumar**, Avaneesh K. Dubey, Priyanka Singh, and R. K. Nagaria, "A High-Speed Energy-Efficient CMOS Dynamic Latch Comparator for Low-Voltage Applications", 6th IEEE Uttar Pradesh Section International Conference on Electrical, Computer and Electronics (UPCON), 8-10 Nov 2019, Aligarh Muslim University, UP, India. **(ISBN- 978-1-7281-3455-0)** 10.1109/UPCON47278.2019.8980209
6. Avaneesh K. Dubey, Pratosh K Pal, Vikrant Varshney, **Ankur Kumar**, and R. K. Nagaria, "Design and Performance of High-speed Low-Offset CMOS Double-Tail Dynamic Comparators using Offset Control Scheme", 9th IEEE Annual International Conference on Information Technology, Electromechanical and Microelectronics (IEMECON), 13-15 March 2019, University of Engineering and Management, Jaipur, India. **(ISBN- 978-1-5386-9325-4)** 10.1109/IEMECONX.2019.8876979

7. **Ankur Kumar**, Vikrant Varshney, Pratosh K Pal, R. K. Nagaria, and Avaneesh K. Dubey, "A Modified High Speed Domino with Low Leakage for Wide Fan-in Domino OR-Gate", 14th IEEE India Council International Conference (INDICON), 16-18 December 2018, Amrita Vishwa Vidyapeetham Coimbatore, India. **(Presented)** **(ISBN-2325-9418)** 10.1109/INDICON45594.2018.8987072
8. Pratosh K Pal, Avaneesh K. Dubey, **Ankur Kumar**, Vikrant Varshney, and R.K.Nagaria, "A 0.55V, 28.6ppm/oC Nanopower Subthreshold Voltage Reference with Body Biasing", 14th IEEE India Council International Conference (INDICON), 16-18 December 2018. Amrita Vishwa Vidyapeetham Coimbatore, India. **(Presented)** **(ISBN-2325-9418)** 10.1109/INDICON45594.2018.8987157
9. Vikrant Varshney, Avaneesh K. Dubey, **Ankur Kumar**, Pratosh K Pal, and R. K. Nagaria, "Design of Power Efficient Low-Offset Dynamic Latch Comparator using 90nm CMOS Process," In 2018 3rd International Innovative Applications of Computational Intelligence on Power, Energy and Controls with their Impact on Humanity (CIPECH),1-2 Nov,2018 pp. 229-233, IEEE, 2018. **(ISBN- 978-1-5386-6472-8)** 10.1109/CIPECH.2018.8724234
10. Manav Bansal, **Ankur Kumar**, Priyanka Singh, R. K. Nagaria, "A Novel 10T SRAM cell for Low Power Applications", 5th IEEE Uttar Pradesh Section International Conference on Electrical, Computer and Electronics (UPCON), 2-4 Nov 2018, MMMUT Gorakhpur, UP, India. **(ISBN- 978-1-5386-5002-8)** 10.1109/UPCON.2018.8596829
11. Vivek Sarswat, **Ankur Kumar**, Pratosh Kumar Pal, R. K. Nagaria, "A Survey on Different Modules of Low-Power High-Speed Hybrid Full Adder Circuits", 4th IEEE Uttar Pradesh Section International Conference on Electrical, Computer and Electronics (UPCON), 26-28 OCT. 2017, GLA University, Mathura, India. **(ISBN- 978-1-5386-3004-4)** **(Presented)** 10.1109/UPCON.2017.8251068
12. Shreyashi, Suchi Nagaria, **Ankur kumar**, R. K. Nagaria, "A Novel Approach for Delay Variation Reduction in Domino Logic Gates using Keeper Circuit", 13th IEEE India Council International Conference (INDICON), 15-17 December 2017. IIT Roorkee, India. **(Presented)** **(ISBN- 978-1-5386-4318-1)** 10.1109/INDICON.2017.8488081
13. **Ankur Kumar**, Sankit R. Kassa, Avaneesh K. Dubey, R. K. Nagaria, and R. K. Singh "Logical Effort Method for Dynamic Power and Delay Estimation of Multi-Threshold CMOS and Its Application in Low Power VLSI", Proc. International Conference on Advance Computational Technique in Information & Communication Technology (ICACTICT-16), KNIT Sultanpur, India, 23-24 September, 2016. **(Presented)** (ISBN-978-93-86256-00-3)
14. Thota Ravi Sankar, Sankit R. Kassa, R. K. Nagaria, and **Ankur Kumar**. "Performance Analysis of Footed Quasi Resistance Scheme for Low Power VLSI Circuits." Proc. IEEE International Conference on Power Electronics, Intelligent Control and Energy Systems (ICPEICES-2016), Delhi Technology University, pp.1-5, 4-6July 2016. **(Presented)** **(ISBN- 978-1-4673-8587-9)** 10.1109/ICPEICES.2016.7853615

Honors and achievements:

- "Best Paper Award" VIth IEEE Uttar Pradesh Section International Conference on Electrical, Computer and Electronics (UPCON-2019) held at Aligarh Muslim University, India.
- "Best Paper Award" IIIrd IEEE Conference on Information and Communication Technology (CICT 2019) held at IIIT Allahabad, UP, India.
- **"GATE** and **NET-JRF"** qualified.

Short-term courses/Workshops/Training Organized:

- A conference on "Advances in Computing and Future Communication Technologies (ICACFCT-2021)" held at Meerut Institute of Engineering and Technology, Meerut, Uttar Pradesh, India during from 16-12-2021 to 17-12-202. **(Organized as Organizing Co-Chair)**
- One-Week FDP on "Emerging Technologies of Opto-VLSI and Its applications" held at Meerut Institute of Engineering and Technology, Meerut, Uttar Pradesh, India during from 31-08-2021 to 04-09-2021. **(Organized as Convener)**
- Webinar on "Advanced VLSI Design Tools for Low Power Applications" held at Meerut Institute of Engineering and Technology, Meerut, Uttar Pradesh, India on 26-12-2020. **(Organized as Moderator)**

Short-term courses/Workshops/Training Attended:

- One-week ATAL FDP on "Research Issues in VLSI Design and Testing" held at Department of Electronics and Communication Engineering, Government College of Engineering Srirangam, Sethurapatti Village, Thiruchirapalli, Tamil Nadu from 02-08-2021 to 06-08-2021.
- One-week ATAL FDP on " VLSI -IP DESIGN Approach to SRAM compiler design" held at Department of Electronics and Communication Engineering, GM Institute of Technology, Davanagere, Karnataka from 16-08-2021 to 20-08-2021.
- One-week STTP on "Innovative & Inventive Problem Solving" held at Department of Electronics and Telecommunication AISSMS COE, Institution of Engineers (India), Kolkata and ISTE, New Delhi from 13-07-2021 to 18-07-2021.
- One-week FDP on "Augment Reality & Virtual Reality" held at Department of Electronics and Telecommunication AISSMS COE, Under IEEE Students Branch, Institution of Engineers (India), Kolkata and ISTE, New Delhi, India during from 21-06-2021 to 25-06-2021.
- One-week FDP on " Recent Trends in Photonics Technology" held at Jaypee Institute of Information Technology, Noida, Uttar Pradesh, India during from 28-12-2020 to 02-01-2021.
- 3-Days FDP on "National Education Policy for Holistic Education and Institutional Ranking" held at Meerut Institute of Engineering and Technology, Meerut, Uttar Pradesh, India during from 10-12-2020 to 12-12-2020.

- One-week STTP on "Emerging Trends in VLSI Design" held at Sardar Vallabhbhai National Institute of Technology Surat during from 12-09-2020 to 16-09-2020.
- One-week FDP on "Artificial Intelligence and Machine Learning Using Python" held at Jaypee Institute of Information Technology, Noida, Uttar Pradesh, India during from 10-08-2020 to 15-08-2020.
- One-week workshop on “Advanced Embedded Systems & Microelectronics” held at MNNIT, Allahabad during from 01-04-2020 to 05-04-2020.
- GIAN course attended on “Advanced in Nanotechnology and Its application in Future Electronics” held at MNNIT, Allahabad during from 06-11-2017 to 10-11-2017.
- One-week workshop on “Mentor Tool Training” held at IIT Kanpur during from 28-01-2017 to 31-01-2017.
- Four Weeks training on “Use of CNC Machine in Manufacturing of Stator Winding” in BHEL, Haridwar.

Place: Una, Himachal Pradesh **ANKUR KUMAR**